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(54) **STRESS REDUCTION APPARATUS**

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(51) **Int. Cl.**

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H01L 29/40	(2006.01)
H01L 25/065	(2006.01)
H01L 21/56	(2006.01)
H01L 23/00	(2006.01)
H01L 23/31	(2006.01)

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CPC ***H01L 25/0657*** (2013.01); ***H01L 21/563*** (2013.01); ***H01L 23/562*** (2013.01); *H01L 23/3192* (2013.01); *H01L 24/13* (2013.01); *H01L 24/16* (2013.01); *H01L 2224/0401* (2013.01); *H01L 2224/05022* (2013.01); *H01L 2224/05572* (2013.01); *H01L 2224/10125* (2013.01); *H01L 2224/13022* (2013.01); *H01L 2224/13111* (2013.01); *H01L 2224/13147* (2013.01); *H01L 2224/14133* (2013.01); *H01L 2224/14135* (2013.01); *H01L 2224/16145* (2013.01); *H01L 2224/73204* (2013.01); *H01L 2225/06513* (2013.01); *H01L 2225/06527* (2013.01); *H01L 2225/06582* (2013.01); *H01L 2924/00014* (2013.01)

(58) **Field of Classification Search**

CPC H01L 23/562
USPC 257/77, E23.026, 777
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

2008/0073784 A1*	3/2008	Lee	....	257/738
2011/0101520 A1*	5/2011	Liu et al.	....	257/737
2011/0210444 A1*	9/2011	Jeng et al.	....	257/738
2011/0260336 A1*	10/2011	Kang et al.	....	257/777

FOREIGN PATENT DOCUMENTS

CN	102376679 A	3/2012
TW	I256117	6/2006
TW	201115703	5/2011

* cited by examiner

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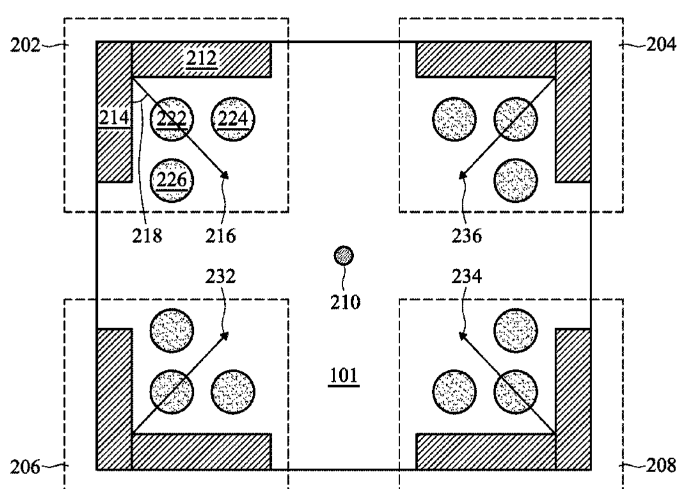
(57) **ABSTRACT**

A structure comprises a plurality of connectors formed on a top surface of a first semiconductor die, a second semiconductor die formed on the first semiconductor die and coupled to the first semiconductor die through the plurality of connectors and a first dummy conductive plane formed between an edge of the first semiconductor die and the plurality of connectors, wherein an edge of the first dummy conductive plane and a first distance to neutral point (DNP) direction form a first angle, and wherein the first angle is less than or equal to 45 degrees.

16 Claims, 4 Drawing Sheets



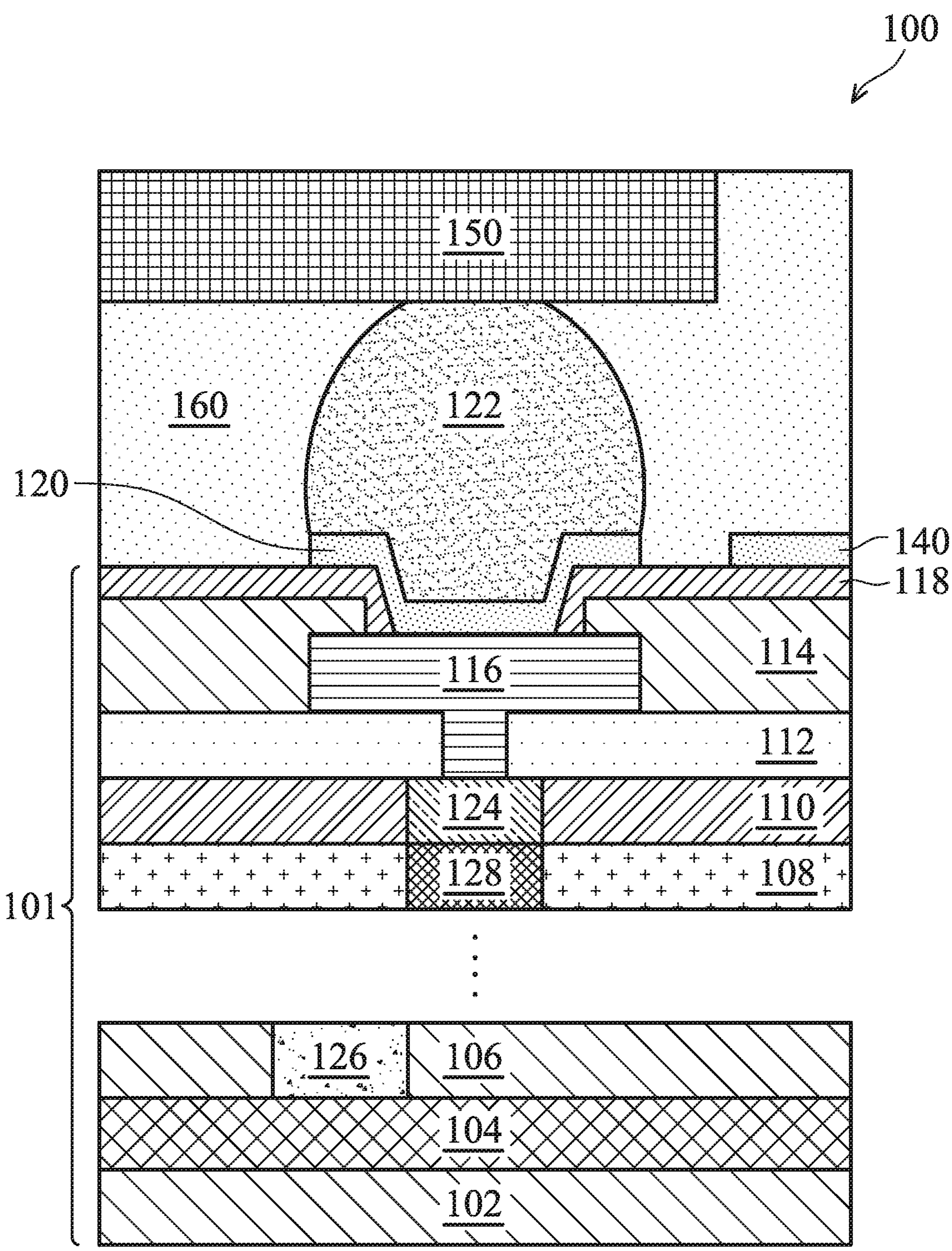

100
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FIG. 1

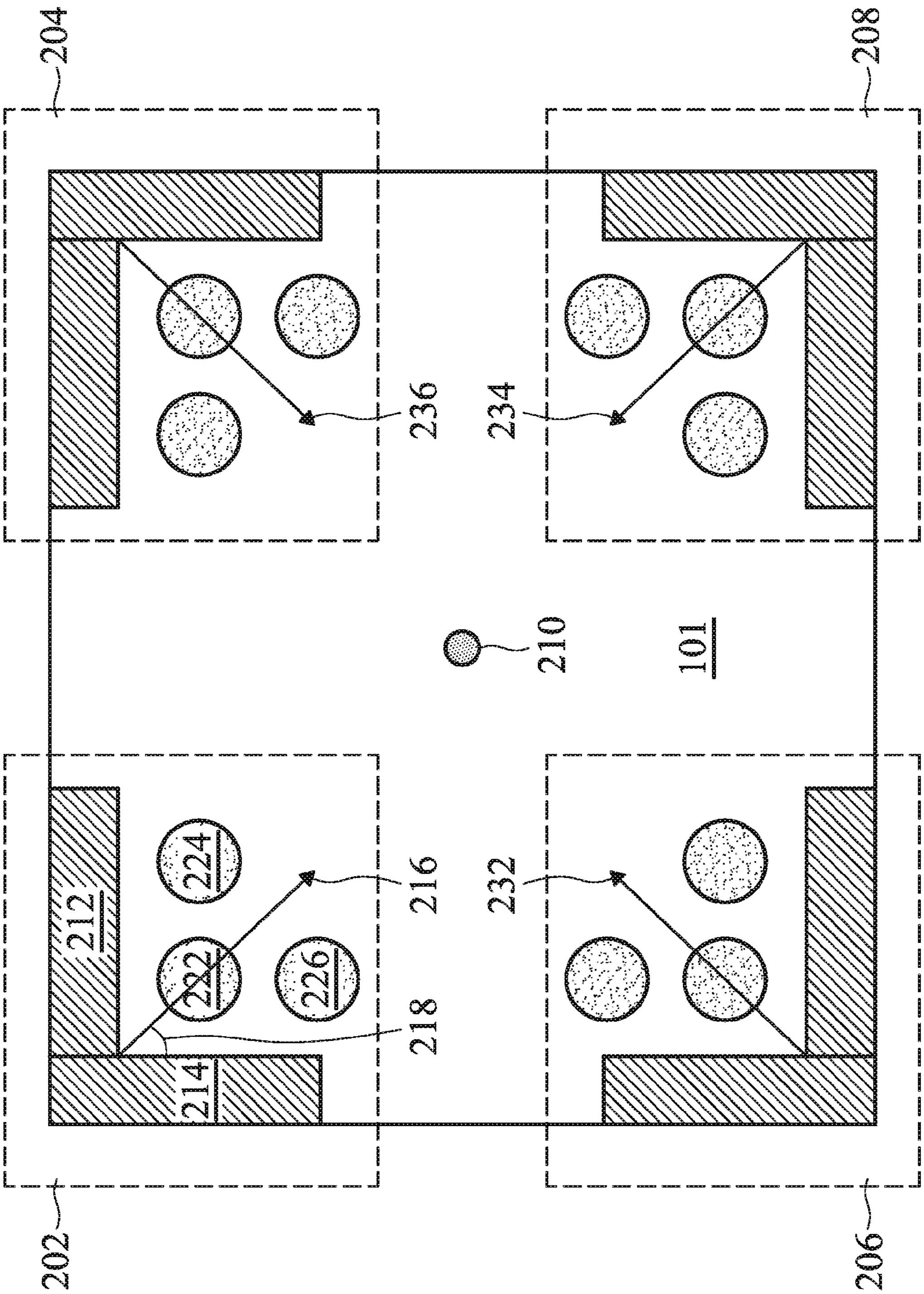
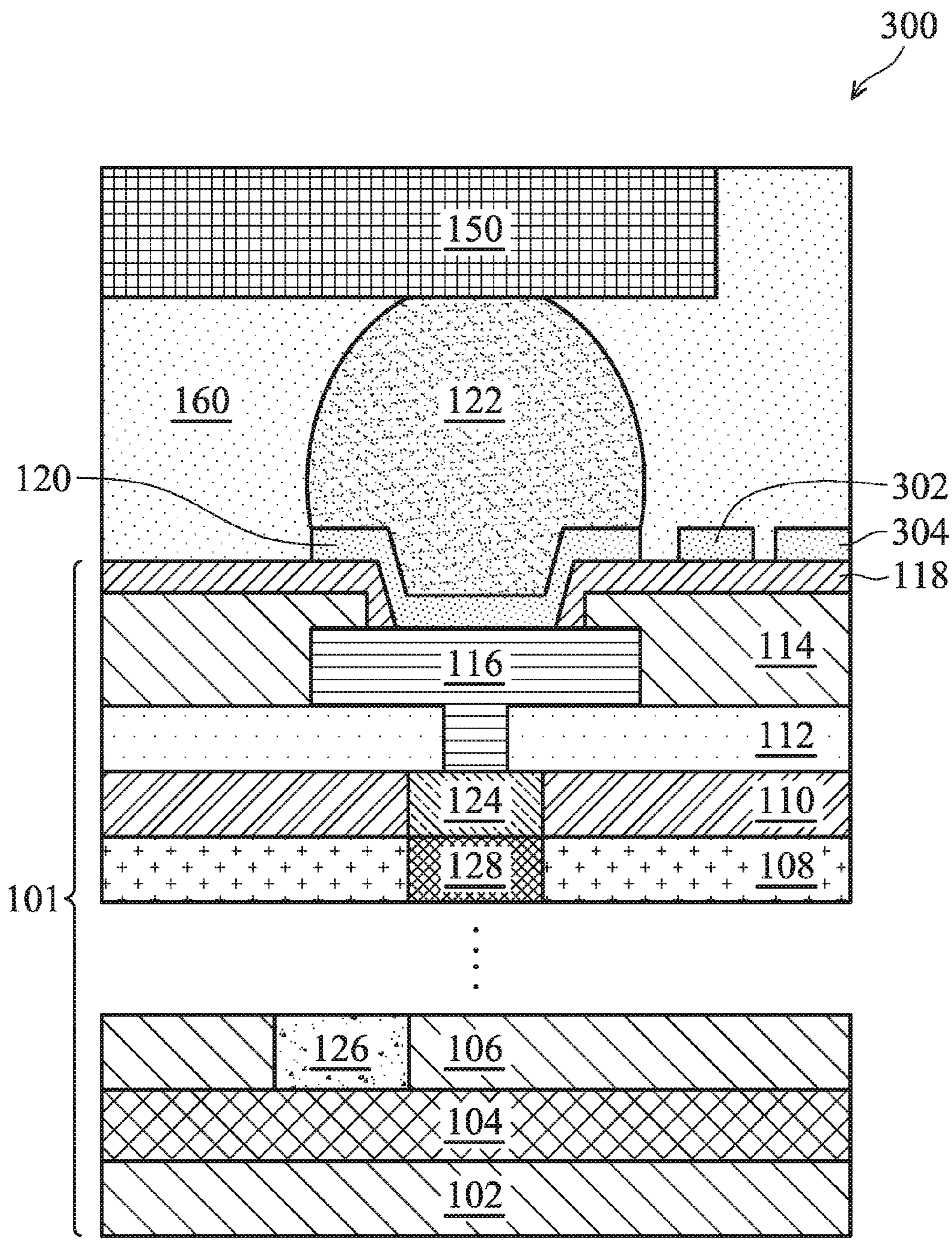


FIG. 2


300
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102

FIG. 3

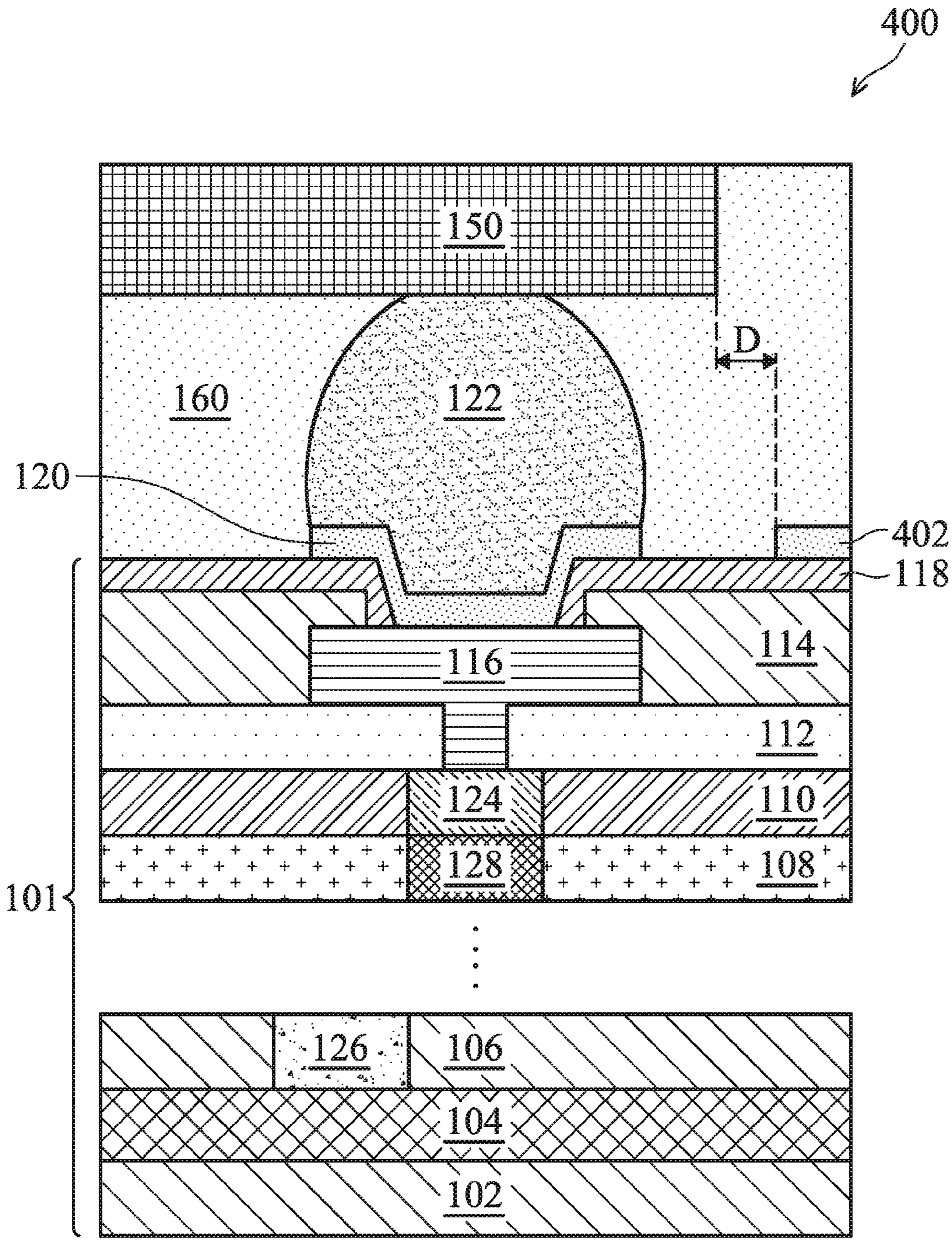
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FIG. 4

STRESS REDUCTION APPARATUS

BACKGROUND

The semiconductor industry has experienced rapid growth due to continuous improvements in the integration density of a variety of electronic components (e.g., transistors, diodes, resistors, capacitors, etc.). For the most part, this improvement in integration density has come from repeated reductions in minimum feature size, which allows more components to be integrated into a given area. As the demand for even smaller electronic devices has grown recently, there has grown a need for smaller and more creative packaging techniques of semiconductor dies.

As semiconductor technologies evolve, three-dimensional integrated circuit devices have emerged as an effective alternative to further reduce the physical size of a semiconductor chip. In a three-dimensional integrated circuit, the packaging is generated on the die with contacts provided by a variety of bumps. Much higher density can be achieved by employing three-dimensional integrated circuit devices. Furthermore, three-dimensional integrated circuit devices can achieve smaller form factors, cost-effectiveness, increased performance and lower power consumption.

A three-dimensional integrated circuit device may comprise a top active circuit layer, a bottom active circuit layer and a plurality of inter-layers. In the three-dimensional integrated circuit, two semiconductor dies may be bonded together through a plurality of bumps and electrically coupled to each other through a plurality of through vias. The bumps and through vias provide an electrical interconnection in the vertical axis of the three-dimensional integrated circuit. As a result, the signal paths between two semiconductor dies are shorter than those in a traditional three-dimensional integrated circuit device in which different semiconductor dies are bonded together using interconnection technologies such as wire bonding based chip stacking packages. A three-dimensional integrated circuit device may comprise a variety of semiconductor dies stacked together. The multiple semiconductor dies are packaged before the wafer has been diced.

The three-dimensional integrated circuit technology has a variety of advantages. One advantageous feature of packaging multiple semiconductor dies at the wafer level is multichip wafer level package techniques may reduce fabrication costs. Another advantageous feature of wafer level package based multi-chip semiconductor devices is that parasitic losses are reduced by employing bumps and through vias.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present disclosure, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. **1** illustrates a cross sectional view of a three dimensional integrated circuit having dummy conductive planes in accordance with an embodiment;

FIG. **2** illustrates a top view of an uppermost surface of the first semiconductor die shown in FIG. **1** in accordance with an embodiment;

FIG. **3** illustrates a cross sectional view of a three dimensional integrated circuit having dummy conductive planes in accordance with another embodiment; and

FIG. **4** illustrates a cross sectional view of a three dimensional integrated circuit having dummy conductive planes in accordance with yet another embodiment.

Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the various embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the presently embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the disclosure, and do not limit the scope of the disclosure.

The present disclosure will be described with respect to embodiments in a specific context, a stress reduction apparatus of a three dimensional integrated circuit. The disclosure may also be applied, however, to a variety of semiconductor devices. Hereinafter, various embodiments will be explained in detail with reference to the accompanying drawings.

FIG. **1** illustrates a cross sectional view of a three dimensional integrated circuit having dummy conductive planes in accordance with an embodiment. As shown in FIG. **1**, the three dimensional integrated circuit **100** includes a first semiconductor die **101** and a second semiconductor die **150** stacked on top of the first semiconductor die **101**. The second semiconductor die **150** may be of a structure similar to the first semiconductor die **101**. For simplicity, only the detailed structure of the first semiconductor die **101** is illustrated in FIG. **1** to show innovative aspects of various embodiments.

The first semiconductor die **101** comprises a substrate **102**. The substrate **102** may be formed of silicon, although it may also be formed of other group III, group IV, and/or group V elements, such as silicon, germanium, gallium, arsenic, and combinations thereof. The substrate **102** may also be in the form of silicon-on-insulator (SOI). The SOI substrate may comprise a layer of a semiconductor material (e.g., silicon, germanium and/or the like) formed over an insulator layer (e.g., buried oxide or the like), which is formed in a silicon substrate. In addition, other substrates that may be used include multi-layered substrates, gradient substrates, hybrid orientation substrates and/or the like.

The substrate **102** may further comprise a variety of electrical circuits (not shown). The electrical circuits formed on the substrate **102** may be any type of circuitry suitable for a particular application.

In accordance with an embodiment, the electrical circuits may include various n-type metal-oxide semiconductor (NMOS) and/or p-type metal-oxide semiconductor (PMOS) devices such as transistors, capacitors, resistors, diodes, photo-diodes, fuses and the like. The electrical circuits may be interconnected to perform one or more functions. The functions may include memory structures, processing structures, sensors, amplifiers, power distribution, input/output circuitry or the like.

One of ordinary skill in the art will appreciate that the above examples are provided for illustrative purposes only to further explain applications of the present disclosure and are not meant to limit the present disclosure in any manner.

An interlayer dielectric layer **104** is formed on top of the substrate **102**. The interlayer dielectric layer **104** may be formed, for example, of a low-K dielectric material, such as silicon oxide. The interlayer dielectric layer **104** may be formed by any suitable method known in the art, such as spinning, chemical vapor deposition (CVD) and plasma enhanced chemical vapor deposition (PECVD). It should also be noted that one skilled in the art will recognize that the interlayer dielectric layer **104** may further comprise a plurality of dielectric layers.

A bottom metallization layer **106** and a top metallization layer **108** are formed over the interlayer dielectric layer **104**. As shown in FIG. **1**, the bottom metallization layer **106** comprises a first metal line **126**. Likewise, the top metallization layer **108** comprises a second metal line **128**. Metal lines **126** and **128** are formed of metal materials such as copper or copper alloys and the like. The metallization layers **106** and **108** may be formed through any suitable techniques (e.g., deposition, damascene and the like). Generally, the one or more inter-metal dielectric layers and the associated metallization layers are used to interconnect the electrical circuits in the substrate **102** to each other to form functional circuitry and to further provide an external electrical connection.

It should be noted while FIG. **1** shows the bottom metallization layer **106** and the top metallization layer **108**, one skilled in the art will recognize that one or more inter-metal dielectric layers (not shown) and the associated metallization layers (not shown) are formed between the bottom metallization layer **106** and the top metallization layer **108**. In particular, the layers between the bottom metallization layer **106** and the top metallization layer **108** may be formed by alternating layers of dielectric (e.g., extremely low-k dielectric material) and conductive materials (e.g., copper).

A dielectric layer **110** is formed on top of the top metallization layer **108**. As shown in FIG. **1**, a top metal connector **124** is embedded in the dielectric layer **110**. In particular, the top metal connector provides a conductive channel between the metal line **128** and the electrical connection structure of the semiconductor device. The top metal connector **124** may be made of metallic materials such as copper, copper alloys, aluminum, silver, gold and any combinations thereof. The top metal connector **124** may be formed by suitable techniques such as CVD. Alternatively, the top metal connector **124** may be formed by sputtering, electroplating and the like.

A first passivation layer **112** is formed on top of the dielectric layer **110**. In accordance with an embodiment, the first passivation layer **112** is formed of non-organic materials such as un-doped silicate glass, silicon nitride, silicon oxide and the like. Alternatively, the first passivation layer **112** may be formed of low-k dielectric such as carbon doped oxide and the like. In addition, extremely low-k (ELK) dielectrics such as porous carbon doped silicon dioxide can be employed to form the first passivation layer **112**. The first passivation layer **112** may be formed through any suitable techniques such as CVD. As shown in FIG. **1**, there may be an opening formed in the first passivation layer **112**. The opening is used to accommodate the bond pad **116**, which will be discussed in detail below.

A second passivation layer **114** is formed on top of the first passivation layer **112**. The second passivation layer **114** may be similar to the first passivation layer **112**, and hence is not discussed in further detail to avoid unnecessary repetition. As shown in FIG. **1**, a bond pad **116** is formed in the openings of the first passivation and second passivation layers. The bond pad **116** may be made of metallic materials such as copper, copper alloys, aluminum, silver, gold and any combinations thereof, and/or multi-layers thereof. The bond pad **116** may be formed by suitable techniques such as CVD. Alternatively, the bond pad **116** may be formed by sputtering, electroplating and/or the like.

The bond pad **116** may be enclosed by the first and second passivation layers **112** and **114**. In particular, a bottom portion of the bond pad **116** is embedded in the first passivation layer **112** and a top portion of the bond pad **116** is embedded in the second passivation layer **114**. The first and second passivation layers **112** and **114** overlap and seal the edges of the bond pad **116** so as to improve electrical stability by preventing the edges of the bond pad **116** from corrosion. In addition, the passivation layers may help to reduce the leakage current of the semiconductor device.

A polymer layer **118** is formed on top of the second passivation layer **114**. The polymer layer **118** may be made of polymer materials such as epoxy, polyimide, polybenzoxazole (PBO), silicone, benzocyclobutene (BCB), molding compounds and/or the like. In accordance with various embodiments, the polymer layer **118** may be formed of PBO. For simplicity, throughout the description, the polymer layer **118** may be alternatively referred to as the PI layer **118**. The polymer layer **118** may be made by suitable deposition methods known in the art such as spin coating and/or the like.

A redistribution layer (not shown) may be formed in the three dimensional integrated circuit **100** if the bond pad **116** is relocated to a new location. The redistribution layer provides a conductive path between the metal lines (e.g., metal line **128**) and the redistributed bond pad. The operation principles of redistribution layers are well known in the art, and hence are not discussed in detail herein.

The PI layer **118** is patterned to form a plurality of openings. Furthermore, various under bump metal (UBM) structures (e.g., UBM **120**) are formed on top of the openings. The UBM structures (e.g., UBM **120**) are employed to connect the bond pads (e.g., bond pad **116**) with various input and output terminals (e.g., connector **122**). The UBM structures may be formed by any suitable techniques such as electroplating. Other processes of formation such as sputtering, evaporation, PECVD and the like may alternatively be used depending upon the desired materials.

As shown in FIG. **1**, there may be a plurality of dummy conductive planes **140** formed on top of the PI layer **118**. The dummy conductive planes **140** are placed between the UBM structures **120** and the edge of the first semiconductor die **101**. In accordance with an embodiment, the dummy conductive planes **140** may be formed of copper. The shape and location of the dummy conductive planes **140** will be described in detail below with respect to FIG. **2**.

The Connector **122** is formed on top of the UBM structure **120**. In accordance with an embodiment, the connector **122** may be a solder ball. The solder ball **122** may be made of any of suitable materials. In accordance with an embodiment, the solder ball **122** may comprise SAC405. SAC405 comprises 95.5% Sn, 4.0% Ag and 0.5% Cu.

In accordance with an embodiment, the connector **122** may be a copper bump. The copper bump may be of a height of approximately 45 um. In accordance with an embodiment, a variety of semiconductor packaging technologies such as sputtering, electroplating and photolithography can be employed to form the copper bump. As known in the art, in order to insure the reliable adhesion and electrical continuity between the copper bump and the bond pad **116**, additional layers including a barrier layer, an adhesion layer and a seed layer may be formed between the copper bump and the bond pad **116**. It should be noted that the connectors shown in FIG. **1** are merely an example. The disclosure is applicable to a variety of semiconductor connectors.

An underfill material layer **160** may be formed in the gap between the top surface of the first semiconductor die **101** and the second semiconductor die **150**. In accordance with an embodiment, the underfill material **160** may be an epoxy, which is dispensed at the gap between the top surface of the first semiconductor die **101** and the second semiconductor die **150**. The epoxy may be applied in a liquid form, and may harden after a curing process.

In accordance with another embodiment, the underfill material layer **160** may be formed of curable materials such as polymer based materials, resin based materials, polyimide, epoxy and any combinations of thereof. The underfill material layer **160** can be formed by a spin-on coating process, dry film lamination process and/or the like. An advantageous feature of having an underfill material (e.g., underfill material **160**) is that the underfill material **160** helps to prevent the three dimensional integrated circuit **100** from cracking during reliability tests such as thermal cycling processes. In addition, another advantageous feature is that the underfill material **160** may help to reduce the mechanical and thermal stresses during the fabrication process of the three dimensional integrated circuit **100**.

FIG. **2** illustrates a top view of an uppermost surface of the first semiconductor die shown in FIG. **1** in accordance with an embodiment. As shown in FIG. **2**, the top surface of the first semiconductor die **101** may include four corners, namely corners **202**, **204**, **206** and **208**. There may be a plurality of connectors (e.g., connectors **222**, **224** and **226**) placed between four corners. In consideration with mechanical strength and design for manufacturing, the connectors (e.g., connector **222**) may not be placed adjacent to the edges of the first semiconductor die **101**. Instead, a plurality of dummy copper planes (e.g., dummy copper planes **212** and **214**) may be placed between the connectors (e.g., connectors **222**, **224** and **226**) and the edges of the first semiconductor die **101**.

The center point of the top surface of the first semiconductor die **101** is referred to as a center point **210**. A first Distance to Neutral Point (DNP) direction **216** is defined as a direction from an upper left corner (e.g., corner **202**) of the top surface of the first semiconductor die **101** to the center point **210** of the first semiconductor die **101**. The starting point of the first DNP direction **216** is the turning point between the dummy copper plane **212** and the dummy copper plane **214**.

Likewise, as shown in FIG. **2**, a second DNP direction **232** is defined as a direction from the bottom left corner (e.g., corner **206**) of the top surface of the first semiconductor die **101** to the center point **210** of the first semiconductor die **101**. The starting point of the second DNP direction **232** is the turning point between the dummy copper planes of the bottom left corner. A third DNP direction **234** is defined as a direction from the bottom right corner (e.g., corner **208**) of the top surface of the first semiconductor die **101** to the center point **210** of the first semiconductor die **101**. The starting point of the third DNP direction **234** is the turning point between the dummy copper planes of the bottom right corner. A fourth DNP direction **236** is defined as a direction from the upper right corner (e.g., corner **204**) of the top surface of the first semiconductor die **101** to the center point **210** of the first semiconductor die **101**. The starting point of the fourth DNP direction **236** is the turning point between the dummy copper planes of the upper right corner.

In accordance with an embodiment, in order to reduce the stress of the region adjacent to the connectors (e.g., connector **222**), the shape and location of dummy conductive planes (e.g., dummy conductive plane **214**) are subject to the following restriction. That is, a DNP direction and the outer edge of its adjacent dummy conductive plane may form an angle, which is less than or equal to 45 degrees. For example, in the upper left corner **202**, there may be two dummy conductive planes **212** and **214**. The outer edge of the dummy conductive plane **214** and the first DNP direction **216** form an angle **218**. In accordance with an embodiment, the angle **218** may be approximately equal to 45 degrees. Alternatively, the angle **218** may be less than 45 degrees.

In a semiconductor device having conventional dummy conductive planes, the angle (e.g., 90 degrees) between the outer edge of a dummy conductive plane and its corresponding DNP direction may exaggerate the stress surrounding the connector adjacent to the dummy conductive plane during thermal cycles or other reliability tests. In particular, the thermal expansion effect during thermal cycles may cause a variety of stresses including tensile stress, compressive stress and/or the like. Such stresses, especially the stress adjacent to the corners of the semiconductor device may cause a variety of corner cracks in the underfill layer over the corners of the semiconductor device. The cracks may extend through the underfill layer and further induce cracks on and in the substrate.

One advantageous feature of having the angle shown in FIG. **2** is that the angle requirement between the dummy conductive plane and the DNP direction helps to reduce the stress so as to prevent corner cracks from occurring.

FIG. **3** illustrates a cross sectional view of a three dimensional integrated circuit having dummy conductive planes in accordance with another embodiment. The three dimensional integrated circuit **300** is similar to the three dimensional integrated circuit **100** shown in FIG. **1** except that the dummy conductive plane **140** shown in FIG. **1** can be replaced by a plurality of dummy conductive planes (e.g., dummy conductive planes **302** and **304**). As shown in FIG. **3**, there may be two dummy conductive planes placed adjacent to the edge of the first semiconductor die **101**. Each dummy conductive plane (e.g., dummy conductive plane **302**) may be of a length in range from about 20 um to about 500 um. It should be noted while FIG. **3** shows two dummy conductive planes, the three dimensional integrated circuit **300** may accommodate any number of dummy planes.

FIG. **4** illustrates a cross sectional view of a three dimensional integrated circuit having dummy conductive planes in accordance with yet another embodiment. The three dimensional integrated circuit **400** is similar to the three dimensional integrated circuit **100** shown in FIG. **1** except that there may be a keep-out zone between the dummy conductive plane **402** and the right edge of the second semiconductor die **150**. As shown in FIG. **4**, the keep-out zone between the dummy conductive plane **402** and the right edge of the second semiconductor die **150** is defined as D. In accordance with an embodiment, D is greater than 50 um.

Although embodiments of the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims.

Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A structure comprising:

a plurality of connectors formed on a top surface of a first semiconductor die;

a second semiconductor die formed on the first semiconductor die and coupled to the first semiconductor die through the plurality of connectors;

a first dummy conductive plane formed between a first edge of the first semiconductor die and the plurality of connectors, wherein the first dummy conductive plane is rectangular in shape and has a long side and a short side, wherein an outer edge of the long side of the first dummy conductive plane is vertically aligned with a first outer edge of the first semiconductor die; and

a second dummy conductive plane formed between a second edge of the first semiconductor die and the plurality of connectors, wherein the second dummy conductive plane is rectangular in shape and has a long side and a short side, wherein an outer edge of the long side of the second dummy conductive plane is vertically aligned with a second outer edge of the first semiconductor die, and wherein the first dummy conductive plane and the second dummy conductive plane form a triangular corner region between the first dummy conductive plane and the second dummy conductive plane, and wherein at least one of the plurality of connectors is located in the triangular corner region.

2. The structure of claim **1**, wherein the plurality of connectors are formed of solder.

3. The structure of claim **1**, wherein the plurality of connectors are formed of copper.

4. The structure of claim **1**, wherein the first dummy conductive plane is formed of copper.

5. The structure of claim **1**, wherein an edge of the first dummy conductive plane is separated from an edge of the second semiconductor die by a horizontal distance, and wherein the horizontal distance is greater than 50 um.

6. The structure of claim **1**, wherein:

the first dummy conductive plane is of a first width from about 20 um to about 500 um.

7. A device comprising:

a substrate comprising silicon;

a first metal layer formed over the substrate;

a second metal layer formed over the first metal layer;

a first passivation layer formed over the second metal layer;

a second passivation layer formed over the first passivation layer;

a bond pad embedded in the first passivation layer and the second passivation layer;

a polymer layer formed on the second passivation layer; and

a connector, a first dummy plane and a second dummy plane formed over the polymer layer, wherein:

the first dummy plane is formed between a first edge of the substrate and the connector, wherein the first dummy plane is rectangular in shape and has a long side and a short side, wherein an outer edge of the long side of the first dummy plane is vertically aligned with an outer edge of the substrate; and

the second dummy plane is formed between a second edge of the substrate and the connector, wherein the second dummy plane is rectangular in shape and has a long side and a short side, wherein an outer edge of the long side of the second dummy plane is vertically aligned with the outer edge of the substrate, and wherein the first dummy plane and the second dummy plane form a triangular corner region between the first dummy plane and the second dummy plane, and wherein the connector is located in the triangular corner region.

8. The device of claim **7**, further comprising a second semiconductor die formed over the substrate and coupled to the substrate through the connector.

9. The device of claim **8**, further comprising an underfill layer formed between a top surface of the substrate and the second semiconductor die, wherein the connector and the first dummy plane are embedded in the underfill layer.

10. The device of claim **9**, wherein the underfill layer is formed of epoxy.

11. The device of claim **7**, wherein the polymer layer comprises polyimide.

12. The device of claim **7**, wherein the bond pad comprises aluminum.

13. The device of claim **7**, further comprising an under bump metallization structure formed over the bond pad.

14. A device comprising:

a polymer layer over a substrate of a first semiconductor die;

an under bump metallization structure formed in the polymer layer;

a connector on the under bump metallization structure;

a second semiconductor die bonded on the first semiconductor die and coupled to the first semiconductor die through the connector;

a first dummy conductive plane on the polymer layer and extending from an outer edge of the first semiconductor die to a first position, wherein the first position is vertically outside an edge of the second semiconductor die, and wherein:

the first dummy conductive plane is rectangular in shape and has a long side and a short side; and

an outer edge of the long side of the first dummy conductive plane is vertically aligned with the outer edge of the first semiconductor die; and

a second dummy conductive plane on the polymer layer and extending from the outer edge of the first semiconductor die to a second position, wherein the first position is vertically outside the edge of the second semiconductor die, and wherein:

the second dummy conductive plane is rectangular in shape and has a long side and a short side; and

an outer edge of the long side of the second dummy conductive plane is vertically aligned with the outer edge of the first semiconductor die, wherein the first dummy conductive plane and the second dummy conductive plane are two sides of a triangular region and the connector is located in the triangular region.

15. The device of claim **14**, wherein:

the first dummy conductive plane and the second dummy conductive plane form an L-shaped region.

16. The device of claim **14**, wherein:

a top surface of the first dummy conductive plane is level with a top surface of the under bump metallization structure.

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